

## REMARKS

The allowance of claims 5-10 is acknowledged appreciatively.

However, the continued rejection of claim 11 under 35 USC 102 for anticipation by the cited Kamei, et al. patent publication continues to be traversed.

The assertion that "Kamei explicitly discloses the attachment of chips (3, 4) to a plate (61) directly by adhesive (Fig. 1; 27, and underfill not labeled; Par, 0038)" correlates devices 3, 4 and plate 61 of the patent publication with chips 22, 24 and plate 23 (Figs. 2a to 2c) of the application. The claimed plate 23 is between the chips 22, 24 and physically connected to the chips directly by adhesive 25. The claimed plate 23 is directly adhesively connected to both chips 22, 24.

In Kamei, paragraph 0033:

The semiconductor-device mounting areas 61, 62, 63, and 64, for mounting the first device 3, the second device 4, the third device 5, and the fourth device 30, respectively, are independently formed.

In Kamei, the plates and chips have a one-to-one correlation, whereby no one plate can be adhered to two chips, as claimed. The Figs. of Kamei are "summarized" and cannot be relied on in any event when contradicted by the text.

Claim 11 includes an adhesive. The Action correlates the adhesive to 27, underfill not identified and, in paragraph 0038 "... adhesive materials ... having thermal fusible adhesive property ... designated ... 19, 22, 24 and 29, in FIG. 1." In other words, the claimed single adhesive is correlated to six adhesives in the Action, which is not anticipation and, at least because unclear, not a basis for obviousness, either.

According to paragraph 0031 of Kamei, the mounting area 61 and the disposing area 6 are parts of the substrate 2, i.e., the mounting area 61 is a substrate that is electrically connected to the disposing area 6, area 13, plate 72 or adhesive agent 73 (which are designated as "substrate" in the Action. In contrast, the plate 23 of the claim is an independent element that is not electrically connected to the substrate. Therefore, at least something does not correlate as suggested in the Action.

Additionally, in Kamei, the first device 3 is mounted to the mounting area by the bumps 19, and is electrically connected to the disposing area 6 through the mounting area 61. In comparison, the first chip 22 claimed is electrically connected to the substrate 21 directly (by flip chip or wire bonding), which does not go through plate 23.

As to the second device 4 of Kamei, it must be mounted to the mounting area 62 so as to be electrically connected to the disposing area 6 through the mounting area 62. Therefore, as taught by Kamei, et al., the stacked structure must have two devices 3, 4 and two respective mounting areas 61, 62, whereas the claimed invention has two chips 22, 24 on one plate 23.

It may be concluded, therefore, that the assertion that the plate 61 (FIG. 2) in the cited Kamei, et al. patent publication is identical to the plate 23 (FIGS. 2a to 2c) of the claims is unreasonable and that it is obvious therefrom, contestable.

Reconsideration and allowance are, therefore, requested.

Respectfully submitted,



William R. Evans  
c/o Ladas & Parry LLP  
26 West 61<sup>st</sup> Street  
New York, New York 10023  
Reg. No. 25858  
Tel. No. (212) 708-1930